REMARKS

Restriction Election

In the Office Action of May 31, 2006 (hereinafter, "Office Action"), a restriction to one of three groups, listed below, is required under 35 U.S.C. 121:

I. Claims 1 – 16, classified in class 713, subclass 2

II. Claims 17 – 21, classified in class 716, subclass 6

III. Claims 22 – 27, classified in class 710, subclass 3

Applicants provisionally elected to prosecute the invention of Group I on May 18, 2006, in a telephone conversation with the Examiner. Applicants confirm by respectfully electing Group I, without traverse.

Claim Rejections under 35 U.S.C. § 103(a)

Claims 1 – 11 and 14 – 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereinafter, "AAPA") in view of Corrigan et al, U.S. Patent 6,772,259 (hereinafter, "Corrigan"). In view of the claim amendments, Applicants respectfully disagree.

Please note that claims 1 - 13 have been amended and claims 14 – 16 have been cancelled, as indicated in the "Claim Amendments" section at the end of this document.

The claim amendments address two novel aspects of Applicants' claimed invention: the manner in which interrupts are serviced and the manner in which the power distribution logic operations for the system in both an unpartitioned and in a partitioned state. Claims 1 – 6 address the interrupt controller logic; claims 7 – 8 and 10 – 13 address the power distribution logic; claim 9 is substantially similar to the original claim 9, and pertains to the manner in which the system changes from a partitioned state to an unpartitioned state.

Interrupt Controller Subsystem

The interrupt controller subsystem is described in the specification, starting generally on page 13, with the heading "Boot Interrupt Steering for Partitionable System", and is more particularly described on page 15, with the introduction of Figures 4A and 4B. Figure 4A depicts the operation of an interrupt controller 122 when the multiprocessor system is unpartitioned; Figure 4B depicts its operation when the system is partitioned.

As shown in Figure 4A, the interrupt controller 122 consists of a first programmable interrupt controller (PIC) 230A and a second PIC 230B. Boot-capable I/O devices 210A send interrupts to the first PIC 230A and boot-capable I/O devices 210B send interrupts to the to the second PIC 230B.

When the system 100 is unpartitioned, the second PIC 230B is inactive. Thus, the system 100 includes a mechanism for steering the interrupts intended for the second PIC 230B to the first PIC 230A, using the signal path 234. Upon receiving an interrupt request from boot-capable devices 210A or 210B, the first PIC 230A sends a processor-interrupting signal 128A to the one or more processors 120A. Also, part of the processor-interrupting signal 128A is diverted (as signal 232A), to be received by a MUX 240. The MUX 240 sends the signal 232A out, as processor-interrupting signal 120B to the one or more processors 120B.

As depicted in Figure 4B, when the system 100 is partitioned, the second PIC 230B is active. (Firmware 150 enables the input signal 224B to the second PIC 230B when the system is partitioned, disables the signal 224B when the system is unpartitioned.) Interrupts from boot-capable I/O devices 210A (in the first domain 118A) send interrupt requests 226A to the first PIC 230A; interrupts from boot-capable I/O devices 210B (in the second domain 118B) send interrupt

requests 226B to the second PIC 230B. The first PIC 230A generates processor-interrupting signal 128A, to be received by the one or more processors 120A. The second PIC 230B generates processor-interrupting signal 232B, to be received by the MUX 240. Since the system 100 is partitioned, the signal 232B passes through the MUX 240, as processor-interrupting signal 228B, to be received by the one or more processors 120B.

Amended claims 1 – 6 describe the interrupt controller subsystem 122 of the system 100. Claim 1 recites a plurality of processors, a first plurality of boot-capable devices, a second plurality of boot-capable devices and an interrupt controller subsystem. As is depicted in Figures 4A and 4B, the interrupt controller subsystem is recited as having a first programmable interrupt controller and a second programmable interrupt controller. The claim recitation that follows is divided into two parts: whether the system is partitioned into a first domain and a second domain or is unpartitioned. The recitation of amended claim 1 follows the depictions of Figures 4A and 4B and the description given above.

Amended claim 2 refers to the way in which the interrupt controller subsystem (122) routes the first processor-interrupting signal (128A) such that a third processor-interrupting signal (228B) is generated to interrupt the second plurality of processors (120B), when the system is not partitioned. In this manner, the second plurality of processors 120B are not unused, but will receive the interrupts, when the system is not partitioned.

Amended claim 3 refers to the way in which the interrupt controller subsystem (122) routes interrupt requests (224B) intended for the second (inactive) PIC (230B) as the signal path (234) to be received by the first PIC (230A) when the system is unpartitioned.

Amended claim 4 refers to the role played by the firmware (150) in enabling or disabling the second interrupt controller (230B). The specification describes the role played by the firmware 150 in initializing the system 100 such that the hardware and operating system software (whether legacy or partition-aware) operates successfully. Some of the operations of the firmware 150 are depicted in the flow diagram of Figure 3, as well as in the descriptions on pages 10 – 13 of the specification. In particular, the firmware enables the input to the second PIC 230B when the system is partitioned and disables the input to the second PIC 230B when the system is unpartitioned (page 16, lines 6 – 8).

Amended claims 5 and 6 refer to the presence of a multiplexer (MUX 240) in the interrupt controller subsystem (122). The MUX 240 determines which input signal (232A or 232B) produces the output signal 228B, depending on whether the system 100 is partitioned or not (page 16, lines 22 – 23). When the system 100 is unpartitioned, the MUX 240 receives only the first processor-interrupting signal (232A). When the system 100 is partitioned, the MUX 240 may receive both the first processor-interrupting signal (232A) and the second processor-interrupting signal (232B). In either case, the second plurality of processors (120B) will receive the interrupt request, as desired.

Power Distribution Logic

The system 100 includes power distribution logic 180 that operates according to whether the system is partitioned or not. Figure 5 shows the power distribution logic 180, which feeds a powergoodreset signal 186 to both domains of the multiprocessor system. The powergoodreset signal 186 is most often associated with turning the system 100 on (page 17, line 29 – page 18, line 13). The system 100 also includes a first domain reset handler (182A) and a second domain reset handler (182B). (Where the system 100 is partitioned into

more than two domains, there would be more domain reset handlers.) These handlers 182 control the two hard reset signals (184A and 184B), one for each domain. The hard reset signals are often associated with rebooting the system 100, and operate differently than the powergoodreset signal. The differences are described in the specification (page 18, lines 24 – 29).

The power distribution logic 180 is described further in Figures 6A and 6B. In Figure 6A, the operation of the power distribution logic 180 is depicted for an N-domain partitioned system; in Figure 6B, the logic 180 is depicted when the system 100 is unpartitioned. In Figure 6A, the system 100 is divided into N partitions, in which each partition has its own domain reset handler. The first domain reset handler (182A) issues a first hard reset signal (184A); the second domain reset handler (182B) issues a second hard reset signal (184B), and so on. Each hard reset signal is to be received by the processor and I/O circuitry for its respective domain. In contrast, a single powergoodreset signal is issued by the first domain reset handler (182A), to be received by all processor and I/O circuitry of the system 100. In other words, the powergoodreset signal is not separately controlled within each domain.

As shown in Figures 6A and 6B, there are N-1 two-input MUXes (192B – 192N), each receiving the first hard reset signal 184A, as well as the hard reset signal for its respective domain. The MUXes 192 are controlled by the partition bit 190, as shown. This allows the power distribution logic 180 to control the hard reset signals, depending on whether the system 100 is partitioned or not.

Amended claims 7, 8, 10, 11, 12, and 13 describe the power distribution logic 180 of the system 100. Amended claim 7 refers to the power good reset signal being received by the first domain and the second domain when the system is partitioned (Figure 5). Amended claim 13 refers to the power good

reset signal being received by the first domain and the second domain when the system is unpartitioned.

Amended claim 8 refers to the separate domain reset handlers, one for each domain. Each domain reset handler separately issues a hard reset to its respective domain when the system is partitioned.

Amended claims 10, 11, and 12 refer to two-input multiplexer receiving the first hard reset and the second hard reset. The multiplexer enables the processor and I/O circuitry of the second domain to be reset when the system is unpartitioned (claim 11). When the system is partitioned, the second domain reset handler can issue its own hard reset signal (claim 12).

Claim 9

In Figure 1, the system 100 is shown as having bits r0 125A and r1 125B. These bits are used to transition the system 100 from a partitioned state to an unpartitioned state (page 7, lines 5 – 10). Amended claim 9 depends from amended claim 1.

Claim Rejections

The above claims were rejected under AAPA and, in the case of claims 13 and 14, in view of Corrigan. AAPA discloses a multiprocessor system which simultaneously supports partitioning into multiple domains. However, AAPA does not disclose, nor does it teach or suggest, the interrupt controller subsystem, as disclosed in Applicants' specification or as recited in amended claims 1 – 6. Nor does AAPA disclose, teach, or suggest the power distribution logic, as disclosed in Applicants' specification or as recited in amended claims 7 – 8 and 10 – 13.

Corrigan discloses an interrupt handler that has separate code portions so that, in a first mode, a first code portion is executed, then a common interrupt

handler is executed; in a second mode, a second code portion is executed, then a common interrupt handler is executed. The first mode may be the system operating in a partitioned state while the second mode may be the system operating in an unpartitioned state. Corrigan does not disclose, nor teach or suggest the interrupt controller subsystem as described in Applicants' specification, as depicted in Figures 4A and 4B, and as recited in amended claims 1 – 6. Further, Corrigan fails to disclose the subject of power distribution logic.

For at least these reasons, Applicants' amended claims 1 – 13 are non-obvious over AAPA in view of Corrigan. Applicants respectfully request reconsideration of the obviousness rejections of claims 1 – 13.

Conclusion

Applicants respectfully request reconsideration of the 103(a) rejections of claims 1 - 13, and allowance of these claims.

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Respectfully Submitted,

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Date

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